Claims

[c1] An integrated circuit comprising:
a first bitline with a plurality of memory cells;
a second bitline with a plurality of memory cells;
a sense amplifier having an inverting terminal coupled to the first bitline and a non-inverting terminal coupled to second bitline; and
a reference voltage selection circuit coupled to the sense amplifier, the reference selection circuit generating either a first reference voltage for reading one of the plurality of memory cells on the first bitline or a second reference voltage for reading one of the plurality of memory cells on the second bitline.

[c2] The integrated circuit of claim 1 wherein the memory cells are ferroelectric memory cells.

[c3] The integrated circuit of claim 1 wherein the reference voltage selection circuit comprises an output terminal coupled to the sense amplifier.

[c4] The integrated circuit of claim 3 wherein the reference voltage selection circuit generates either the first or second reference voltage at the output terminal for reading one of the plurality of memory cells on the first or second bitline.

[c5] The integrated circuit of claim 4 wherein the reference voltage selection circuit comprises a first reference generator for generating the first reference voltage and a second reference voltage generator for generating the second reference voltage.

[c6] The integrated circuit of claim 5 further comprises:
a first switch, the first switch selectively couples the first reference generator to the output of the reference voltage selection circuit; and
a second switch, the second switch selectively couples the second reference generator to the output of the reference voltage selection circuit.

[c7] The integrated circuit of claim 6 wherein the first and second switches are transistors.

[c8] The integrated circuit of claim 3 wherein the reference voltage selection circuit

further comprises a select control circuit, the select control circuit receives input information and controls the first and second switches.

[c9] The integrated circuit of claim 8 wherein the input information comprises addressing information.

[c10] The integrated circuit of claim 8 wherein the input information comprises the least significant bit of the address.

[c11] The integrated circuit of claim 3 wherein the reference voltage selection circuit further comprises a select control circuit, the select control circuit receives input information and causes the reference selection circuit to generate the first or second reference voltage.

[c12] The integrated circuit of claim 11 wherein the input information comprises addressing information.

[c13] The integrated circuit of claim 11 wherein the input information comprises the least significant bit of the address.

[c14] The integrated circuit of claim 1 wherein the reference voltage selection circuit comprises a first reference generator for generating the first reference voltage and a second reference voltage generator for generating the second reference voltage.

[c15] The integrated circuit of claim 14 further comprises:
a first switch, the first switch selectively couples the first reference generator to the sense amplifier to provide the sense amplifier with the first reference voltage; and
a second switch, the second switch selectively couples the second reference generator to the sense amplifier to provide the sense amplifier with second reference voltage.

[c16] The integrated circuit of claim 15 wherein the first and second switches are transistors.

[c17] The integrated circuit of claim 16 wherein the reference voltage selection circuit

further comprises a select control circuit, the select control circuit receives input information and controls the first and second switches.

[c18] The integrated circuit of claim 17 wherein the input information comprises addressing information.

[c19] The integrated circuit of claim 17 wherein the input information comprises the least significant bit of the address.

[c20] The integrated circuit of claim 14 wherein the reference voltage selection circuit further comprises a select control circuit, the select control circuit receives input information and causes the reference selection circuit to provide the first or second reference voltage.

[c21] The integrated circuit of claim 20 wherein the input information comprises addressing information.

[c22] The integrated circuit of claim 20 wherein the input information comprises the least significant bit of the address.